AMENDMENTS TO THE CLAIMS

Please amend the claims as shown below:

Claim 1 (Currently Amended). A DC-DC converter that converts a first DC voltage to a second DC voltage comprising:

a first output configured to control a first switch connected to an input of the first DC voltage;

a second output configured to control a second switch, wherein the first and second switches are controlled by ~~an~~ respective first and second input ~~signal~~ signals to generate the second DC voltage;

a sensing device configured to receive a sense signal representative of a current through one of the first or second switches ~~for sensing a current level difference in the second switch~~; and

a control circuit to selectively control at least one of a first delay time between disabling the first switch and enabling the second switch or a second delay time between disabling the second switch and enabling the first switch responsively to the sense signal~~of the input signal by monitoring the current level difference~~.

Claim 2 (Currently Amended). The DC-DC converter of claim 1, wherein the control circuit ~~controls~~ includes a delay circuit and wherein the control circuit is configured to receive a PWM input and delay the first delay time before forming an active state of the first signal and wherein the control circuit is configured to receive the PWM input and delay the second delay time before forming an active state of the second signal.

Claim 3 (Original). The DC-DC converter of claim 2, wherein the delay circuit comprises a charge controlled delay circuit.

Claim 4 (Original). The DC-DC converter of claim 2, wherein the delay circuit comprises a digital controlled delay circuit.

Claim 5 (Currently Amended). The DC-DC converter of claim 1, wherein the sensing device ~~comprises a MOSFET device~~ is configured to receive the sense signal and responsively form a first current sense signal and a second current sense signal wherein the first and second current sense signals are representative of the sense signal and wherein the sensing device is configured to store a value of the first current sense signal and compare the stored value to a value of the second current sense signal to determine the second delay time.

Claim 6 (Original). The DC-DC converter of claim 1, wherein the second switch comprises a power MOSFET device.

Claim 7 (Currently Amended). The DC-DC converter of claim 6, wherein the sensing device senses current conduction of ~~the~~ a body diode of the second switch.

Claim 8 (Currently Amended). A synchronous DC-DC converter structure comprising:

a high-side MOSFET switch having a drain coupled to an input DC voltage and a source coupled to a switch node;

a low-side MOSFET switch having a drain coupled to the switch node and a drain coupled to a ground node;

a sensing device having a drain coupled to the switch node for forming a current sense signal representative of ~~sensing~~ current in the low side MOSFET switch; and

a control structure ~~coupled to the sensing device for monitoring a sensed current difference and adjusting~~ configured to selectively adjust a delay time ~~for~~ between turning ~~on~~ off one of the high-side MOSFET switch and the low-side MOSFET switch and turning on the other of the high-side MOSFET switch and the low-side MOSFET switch.

Claim 9 (Currently Amended). The structure of claim 8, wherein the control structure is coupled to an adjustable delay circuit ~~that increases and decreases the delay time~~ and wherein the control structure is configured to form a first current sense signal and a second current sense signal that are representative of the current sense signal and wherein the control circuit is further configured to store a value of the first current sense signal and compare the stored value to a value of the second current sense signal to selectively adjust the delay time.

Claim 10 (Currently Amended). The structure of claim 9 wherein the adjustable delay circuit comprises a ~~DCD~~ digital controlled delay circuit.

Claim 11 (Currently Amended). The structure of claim 9 wherein the delay circuit comprises a ~~CCD~~ charge controlled delay circuit.

Claim 12 (Original). The structure of claim 8, wherein the sensing device comprises a MOSFET device.

Claim 13 (Original). The structure of claim 8, wherein the sensing device senses body diode current conduction in the low-side MOSFET switch.

Claim 14 (Original). The structure of claim 8, wherein the sensing device senses cross conduction current in the low-side MOSFET switch.

Claim 15 (Currently Amended). A method for controlling delay time in a synchronous DC-DC converter having a high-side switch coupled to a low-side switch comprising the steps of:

forming a first current representative of ~~sensing~~ a current ~~level difference~~ in the low-side switch; and

selectively controlling a delay time ~~in~~ between turning ~~on~~ off one of the high-side switch and the low-side switch and turning on the other of the high-side switch and the low-side switch responsively to the current sense signal~~using the current level difference~~.

Claim 16 (Currently Amended). The method of claim 15 wherein the step of selectively controlling the delay time includes increasing the delay time.

Claim 17 (Currently Amended). The method of claim 15 wherein the step of selectively controlling the delay time includes decreasing the delay time.

Claim 18 (Currently Amended). The method of claim 15 wherein the step of ~~sensing the current level difference~~ forming the first current includes sensing current in the low-side switch with a MOSFET device, forming a first current sense signal and a second current sense signal that are representative of the first current, storing a value of the first current sense signal, and comparing ~~a first current~~

~~level to a second current level to generate the current level difference~~ the stored value and the second current sense signal.

Claim 19 (Currently Amended). The method of claim 15, wherein the step of controlling the delay time includes controlling the delay time with a ~~DCD~~ digital controlled delay circuit.

Claim 20 (Currently Amended). The method of claim 15, wherein the step of controlling the delay time includes controlling the delay time with a ~~CCD~~ charge controlled delay circuit.